DEPARTMENT OF ELECTRONIC & COMMUNICATION ENGINEERING

A Report on

A 5 Day Workshop on Digital VLSI Design Flow Using Xilinx Vivado

(06th February to 10th February 2023)

Department of ECE successfully conducted 5 day workshop on "Digital VLSI Design Flow Using Xilinx Vivado" for 4th B.Tech students from 06th February to 10th February 2023. The objective of this workshop is to provide an overview on Xilinx Vivado ML Enterprise Edition tools for Digital VLSI design using Verilog HDL. The workshop is a live demonstration of Vivado tools by Mr. Pradeep John as resource person from Apply-Volt.

The participants will have exposure to the state-of-the-art VLSI design &FPGA tools for modeling the integrated circuits. At the end of this workshop, the participants will be able to design, verification, implementation and validation of various digital hardware logic blocks.

Total 25 students and 5 faculty members were registered for the workshop and participation certificates for all 30 issued by the department.

Faculty Coordinators: Dr.B. HariPrasad Naik & Mr. A. Aravind

Day-1:

After inaugural session, Director and Head of the Department addressed the faculty and student participants about the importance of workshop and the use of latest Xilinx Vivado tool for designing the hardware logical blocks.

Resource person from Apply Volt, gave a brief overview on various design abstractions such as gate level, data flow and behavioral using Verilog HDL programming.

Day-2:

The day started with the design and implementation of basic logic gates in Xilinx Vivado tool. Different levels of design abstractions such as structural, data-flow and behavioral models were implemented using Verilog HDL in Vivado. Further, the design procedure for synthesizing the hardware designs was explained.

Afternoon session, a complete hands-on session was conducted for writing a test bench program using Verilog HDL. These test bench programs enable the designer to test or simulate the designed hardware logics.

Day-3:

On day three, concept of multiplexers, decoders, encoders, Adders, Multipliers, and their applications in VLSI design was explained in detail.

Afternoon, a hands-on session was conducted for designing, implementation, synthesis, and verification of hardware sub-systems such as encoders, multiplexers, decoders, adders, and using Xilinx Vivado tool. Realization of a hardware on Xilinx Artix-7 FPGA development board was also demonstrated.

Day-4:

On fourth day, the design procedure for designing a higher order systems such as 64-bit Adder and Subtractor with the concept of VIO (Virtual Input and Output) and ILA(Integrated Logic Analyzer) was explained with an example.

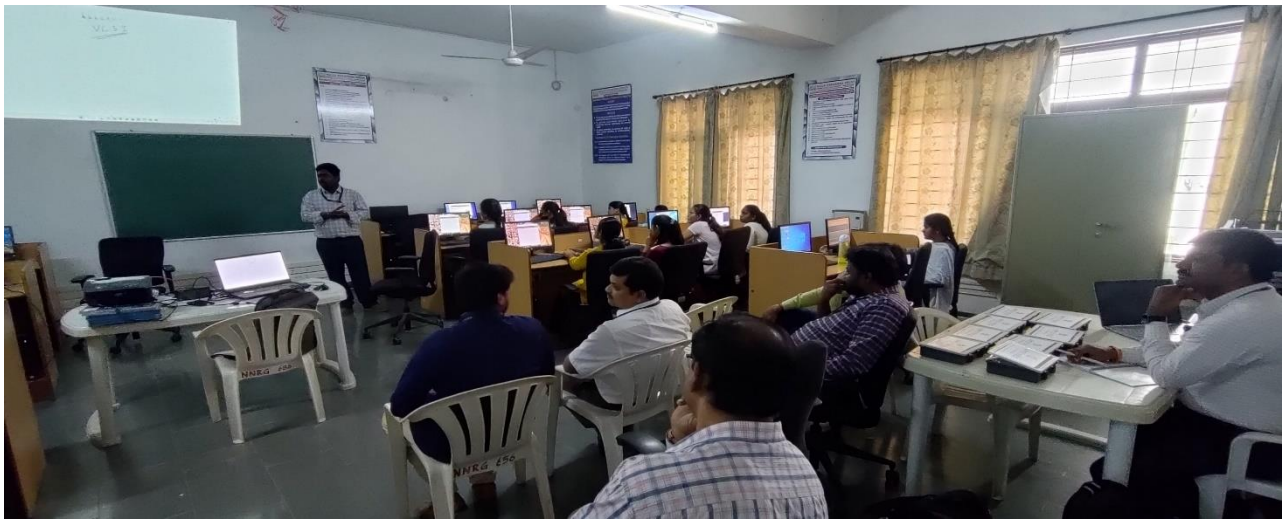
Afternoon, a complete session for hardware realization on Zynq-7000 SoC development board was also demonstrated using Xilinx Vivado tool.

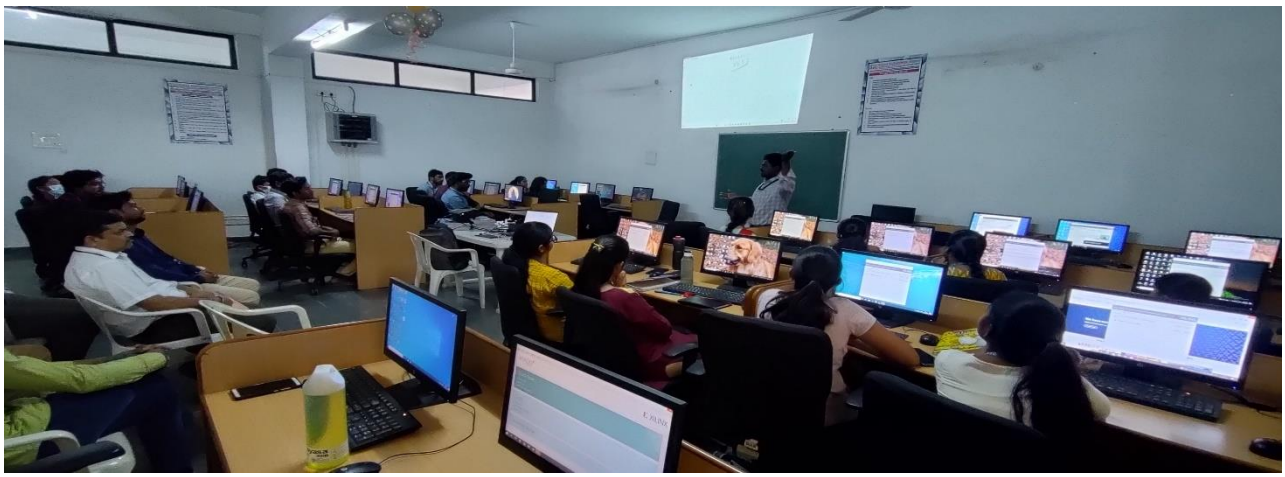
Day-5:

On fifth day; concept and usage of Intellectual Propert (IP) Cores for designing a complex hardware with VIO and ILA using Xilinx Vivado was explained with an example.

In the valedictory session, speakers were facilitated and a vote of thanks was presented by workshop coordinator. Workshop certificates were provided to the participants.

Glimpse of the Workshop:



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